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# Description

# ECHO CANCELLATION DEVICE FOR FULL DUPLEX COMMUNICATION SYSTEMS

## BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The invention generally relates to a full duplex communication system, and more particularly, to an echo cancellation device for a full duplex communication system.

[0003] 2. Description of the Prior Art

[0004] As technology advances, network usage is more and more popular. The requirement of network bandwidth is increasing and the transmission speed of data packets of Ethernet has risen from 10/100Mps to 1Gbps.

[0005] Please refer to FIG. 1, which is a block diagram of a 1 Gbps fast Ethernet system. In the 1 Gbps Ethernet system, each port has 4 channels 100 where each channel has a transceiver 102 and a line interface 116 electrically coupled to a twisted line 118. The transceiver 102 has a

transmitter 104 and a receiver 106, wherein the transmitter 104 has a digital-to-analog converter (DAC) 108 to convert signals into analog form for transmitting to a far-end network device via the line interface 116 and the twisted line 118, and the receiver 106 has an analog front end (AFE) circuit for processing the received signal from the line interface 116 and an analog-to-digital converter (ADC) 114 for converting the processed signals into digital signals and then sending to the after circuits. The fast Ethernet and the far-end network device both simultaneously utilize the four channels where each channel simultaneously performs the transmitting and receiving operations. As a result, the fast Ethernet system is a full duplex communication system.

[0006] Each channel of the fast Ethernet system simultaneously performs the transmitting and receiving operations. When the channel is transmitting, the signals received from the channel are affected by the transmission and this phenomenon is known as echo impairment. In order to reduce echo impairment, an echo cancellation device 110 and an echo cancellation resistor Rp are usually disposed in the transmitter 104 as illustrated in FIG. 1. The echo cancellation device 100 is usually a digital-to-analog converter

(DAC) to output a cancellation signal that is similar to the output signal from the DAC 108 so the cancellation signal can cancel the adverse effects on the receiver 106 by the transmitted signals to achieve echo cancellation.

[0007] Please refer to FIG. 2, which is an equivalent circuit of the fast Ethernet device in FIG. 1. The circuit equivalence of the DAC 108 and the echo cancellation device 110 of the transmitter 104 are current sources Id and Ic respectively. For the receiver 106 to achieve echo cancellation, the output of the current sources Ic and Id must cancel the adverse effects caused by the transmitter 106.

[0008] Please refer to FIG. 3, which is a model of the equivalent circuit in FIG. 2. Zo is the effective output impedance which in FIG. 2 includes a matching resistor Rm for matching impedance and an effective resistor Rc of the channel. Vo is the output signal which is the transmitted signal from the transmitter 104 and is also the received signal from the receiver 106. From the circuit in FIG. 3, we can draw the following formula:

[0009]
$$Vi = \frac{-Zi\left[IdZo + (Zo + Rp)Ic\right]}{Rp + Zi + Zo}$$

(1)

[0010] in order to cancel echo, set vi=0, which satisfies:

[0011] $$IdZo + (Zo + Rp)Ic = 0$$

(2)

[0012] therefore the relationship between Ic and Id is:

[0013] $$Ic = \frac{-Zo}{Rp + Zo} Id$$

(3)

[0014] to accomplish echo cancellation.

[0015] The disadvantages of conventional echo cancellation device is that the effective output impedance Zo is seen as a pure load resistor Re, where the resistance characteristics are based on the matching resistor Rm and the effective resistor Rc. Besides the matching resistor Rm and the effective resistor Rc of the channel, the effective output impedance is also affected by the parasitic capacitance Ce that is unavoidable during operation of the circuit. If the effective output impedance is seen purely as a load resis-

tor Re, echo cancellation cannot be effectively reduced to the lowest.

## SUMMARY OF INVENTION

[0016] It is therefore one of the objects of the claimed invention to provide an echo cancellation device for a full duplex communication system that can effectively cancel echo impairment to solve the above-mentioned problem.

[0017] According to the claimed invention, an echo cancellation device for a full duplex communication system is provided. The full duplex communication system comprises a transmitter for transmitting a transmit signal and a receiver for receiving a receive signal. The echo cancellation device comprises: a filter for filtering the transmit signal; at least an echo cancellation resistor electrically coupled to the transmitter, the receiver, and the echo cancellation device; and an echo residue detection circuit for generating a control signal to control the filter according to the echo residue.

[0018] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

## Brief Description of Drawings

[0019] FIG.1 is a block diagram of a 1 Gbps fast Ethernet device according to the embodiment of the present invention.

[0020] FIG. 2 is an equivalent circuit of the fast Ethernet device in FIG. 1.

[0021] FIG. 3 is a small signal model for the equivalent circuit in FIG. 2.

[0022] FIG. 4 is a block diagram of the fast Ethernet device according to the embodiment of the present invention.

[0023] FIG. 5 is a schematic diagram of the digitally implemented low pass filter in FIG. 4.

[0024] FIG. 6 is a schematic diagram of the analogly implemented low pass filter in FIG. 4.

[0025] FIG. 7 is a block diagram of the fast Ethernet device according to another embodiment of the present invention.

## Detailed Description

[0026] Please refer to FIG. 3, the present invention takes into consideration the unavoidable parasitic capacitance in a practical circuit. The effective output impedance Zo is the parallel of the parasitic capacitance Ce and the load resistor Re, which is made up of the matching resistor Rm and the channel effective resistor Rc. The effective output

impedance Zo is calculated by the following equation:

[0027]

$$Zo = \frac{Re}{s\,Re\,Ce + 1}$$

(4)

[0028] substitute formula (4) into formula (3) to obtain formula (5):

[0029]

$$Ic = \frac{-Re}{Rp + Re + s\,Re\,Rp\,Ce}\,Id = H(s) \cdot Id$$

(5)

[0030] From formula (5), it is known that the relationship between Ic and Ic is defined by a low pass transfer function. Please refer to FIG. 4, which shows a block diagram of the fast Ethernet device according to the first embodiment of the present invention. The echo cancellation device of the embodiment of the present invention comprises: an echo cancellation circuit 410 for generating a cancellation signal that corresponds to the transmit signal from the DAC 408; an echo cancellation resistor Rp electrically coupled between the transmitter 404 and the receiver 406; and a low pass filter 420 electrically coupled to the echo cancel-

lation circuit 410 as a front-end circuit. The echo cancellation circuit 410 can be a DAC and the low pass filter 420 can be implemented either analogly or digitally. The digital low pass filter 420 is shown in FIG. 5 and the analog low pass filter 420 is the RC network low pass filter which is shown in FIG. 6. The low pass filter 420 allows the cancellation signal outputted by the echo cancellation circuit 410 to cancel the transmit signal from the DAC 408 (the current source Id in the circuit) so echo impairment of the receiver 406 is reduced to a minimum. The capacitor in FIG. 6 can be a metal-stacked layer capacitor or a parasitic capacitor and the resistor can be a MOS transistor where the equivalent resistance of the MOS transistor is controlled by the Vd of the gate electrode.

[0031] Please refer to FIG. 7, which is a block diagram of the fast Ethernet device according to a second embodiment of the present invention. In practical operation, the capacitance of the parasitic capacitor Ce, the channel effective resistor Rc, and the impedance matching resistor Rm are affected by the operating environment, temperature, manufacturing deviations, and the like, therefore the values will fluctuate and change when transmitting/receiving data. In order to more precisely eliminate echo, in the second em-

bodiment of the present invention, the receiver 706 further comprises an echo residue detection circuit 722 for detecting the amount of echo residue at the receiver 706. The echo residue detection circuit 722 outputs a control signal to the low pass filter 720 according to the detected echo residue to form a loop. The digitally implemented low pass filter 720 takes the adjustment of the coefficients of a finite impulse response (FIR) or a infinite impulse response (IIR) and the analogly implemented low pass filter 720 takes the adjustment of the RC value of the low pass RC filter by controlling the gate voltage Vd to actively adjust the low pass filter 720 according to the different characteristics of circuit components and network environment to maintain the best echo cancellation performance.

[0032] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, that above disclosure should be construed as limited only by the metes and bounds of the appended claims.